

The Design of Fault Tolerant Quantum Dot Cellular Automata Based Logic

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Abstract

As transistor geometries are reduced, quantum effects begin to dominate device performance. At some point, transistors cease to have the properties that make them useful computational components. New computing elements must be developed in order to keep pace with Moore's Law. Quantum dot cellular automata (QCA) represent an alternative paradigm to transistor-based logic. QCA architectures that are robust to manufacturing tolerances and defects must be developed. We are developing software that allows the exploration of fault tolerant QCA gate architectures by automating the specification, simulation, analysis and documentation processes.

1. Introduction

University of Notre Dame researchers [Lent et al.] designed the first quantum dot cellular automata (QCA) logic gates in the early 1990's [1-9, 11]. The operation of these QCA logic gates was verified using large lithographically defined devices. However, the proper operation of these logic gates is strongly dependent on precise manufacturing. Due to their large size, these devices had to be operated at cryogenic temperatures in order for the quantum mechanical effects to be observed. In order to achieve room temperature operation, the quantum dot diameter had to be reduced to approximately 10nm. At this size it is extremely difficult to achieve the required manufacturing tolerances. In order for QCA-based logic to be viable, QCA gate architectures that are robust to manufacturing variations and defects must be developed.

2. Fault Tolerance of the QCA Majority Gate

The family of universal gates for QCA-based logic is composed of the majority gate and the inverter. The majority gate is a three input, single output device that responds according to the rules given in Table 1 [1, 2].

Preliminary investigations of the performance of the ideal majority gate (Figure 1) revealed that the performance of the ideal majority gate is insensitive to certain types of errors in cell position and extremely sensitive to others. For example, a symmetrical rotation of up to 45° of the inputs and output around the central cell (Figure 2) does not affect the performance of the majority gate. Similarly, linear translation of inputs of up to 20 nm along their axes (Figure 3) does not affect the performance of the majority gate.

Table 1 Majority Gate Truth Table

Inputs			Output
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

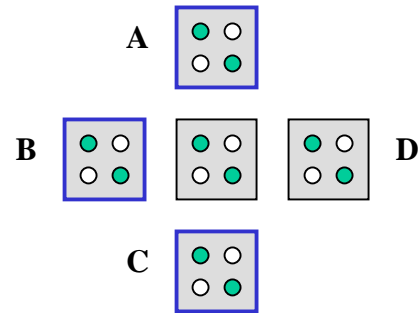


Figure 1 Ideal QCA Majority Gate

However, when the translation in position is not symmetrical, the acceptable position error is significantly reduced. The acceptable error scales with QCA cell size. The maximum error is less than one-half of a QCA cell side (Figure 4).

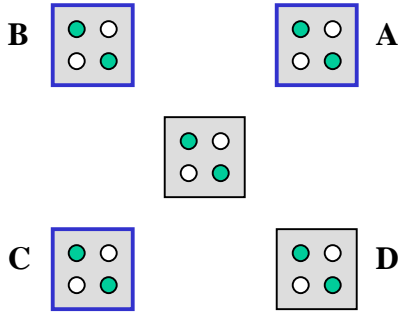


Figure 2 45° Symmetrical Rotation of IO

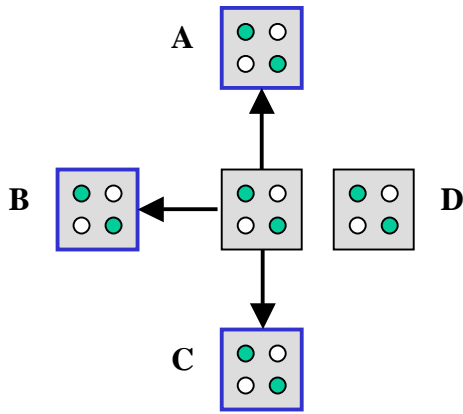


Figure 3 Linear Translations of Inputs

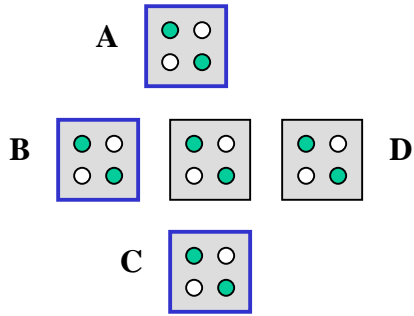


Figure 4 Asymmetrical Errors in Cell Position Cause Failure

The block majority gate architecture (Figure 5) was developed to provide a majority gate that is robust to manufacturing induced errors in cell position, missing cells and defective cells [10, 12]. Preliminary simulation results demonstrate that this architecture provides a significant improvement in the robustness of the ideal majority gate. Research is on-going to quantify this improvement and determine the optimal configuration.

3. AQUINAS

The core of the QCA simulation system is the A Quantum Interconnected Network Array Simulator (AQUINAS) developed by Lent et al [14]. AQUINAS implements the Hartree-Fock approximation to model the quantum mechanical behavior of the quantum dots and the QCA cells. AQUINAS utilizes three different algorithms to simulate the time evolution of the state of an array of QCA cells in response to external inputs. The Crank-Nickolson algorithm solves the time-dependent Schrodinger equation. The spectral decomposition algorithm represents the initial state of a system as a linear combination of stationary states. The time evolution of each stationary state is calculated and superposition is used to calculate the final state of the system. The adiabatic marching algorithm changes the system's inputs according to their time dependence and the ground state is recalculated for each time step.

However, statistical analysis is required to fully explore the fault tolerance of QCA gate architectures [13]. This requires the creation, execution and analysis of a large number of simulations. AQUINAS does support command line driven simulation, however, AQUINAS does not support the generation and analysis of statistical data sets. To add this capability we are integrating AQUINAS into a framework (Figure 6) that will enable Tolerance Optimization using Modern design of

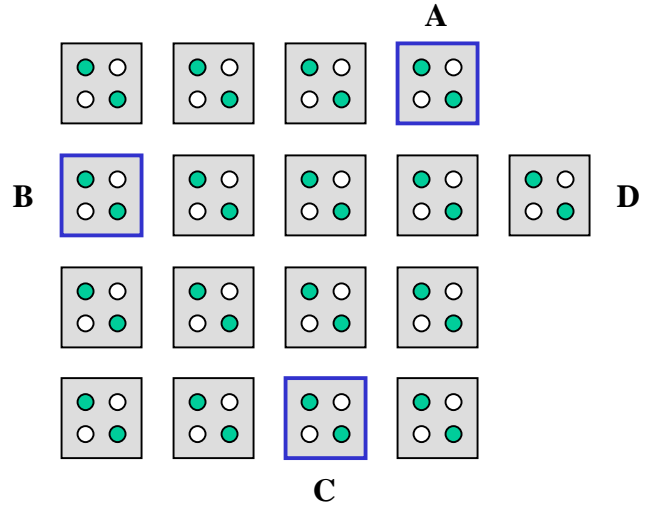


Figure 5 QCA Block Majority Gate

experiment AnalyseS (TOMAS). The TOMAS AQUINAS framework will incorporate of a series of existing software packages (Condor, AQUINAS, and MATLAB Report Generator) with custom software developed specifically for this program.

4. TOMAS AQUINAS Front End Tools

The TOMAS AQUINAS front-end tools provide all of the functionality of the AQUINAS interface plus the enhanced functionality required to perform a quantitative statistical analysis of the fault tolerance of QCA gate architectures. In order to achieve this, two software modules are being created and integrated with a third to create the front end of the TOMAS AQUINAS framework:

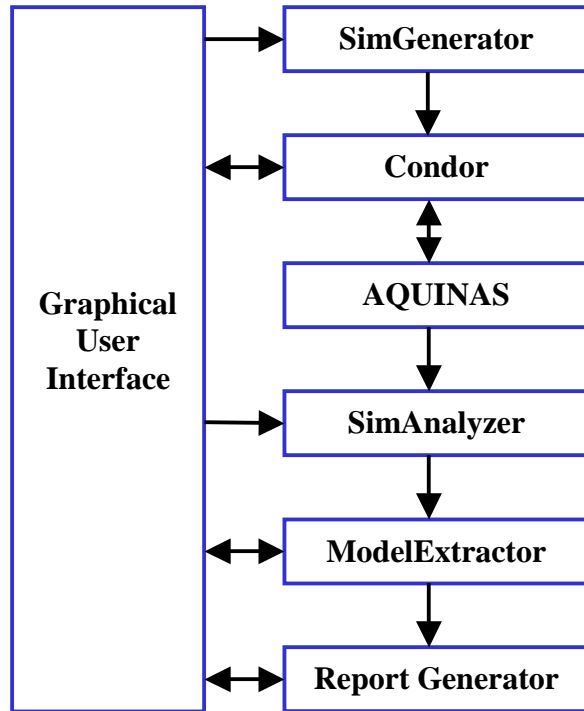


Figure 6 Block Diagram of TOMAS AQUINAS

A new graphical user interface (GUI) provides a single hierarchical interface to all of the tools integrated into the TOMAS AQUINAS framework. The GUI captures all of the information required by the other tools and stores this information in a configuration file. The other programs in the TOMAS AQUINAS framework interact with the GUI through function calls and accessing the configuration file.

SimGenerator allows the user to specify the statistical distribution, mean and variance for several types of manufacturing errors and defects, and apply that distribution to the elements of the gate being studied. The user can model errors in both the x- and y-position of cells relative to the ideal position. The distribution of missing cells and defective cells can also be modeled. The user specifies the number of files to generate and SimGenerator creates a Monte Carlo simulation file set.

SimGenerator can be used iteratively to create a series of Monte Carlo simulation file sets with different parameters.

Condor [17] is a free software package used to configure, control and monitor the batch processing of the Monte Carlo simulation files. Condor allows the user to specify the files to run and configure the available computational resources. Condor automatically distributes the jobs among the available computational resources and launches the simulations. Condor tracks each job, automatically load balances the system, and can even reinitiate a simulation if the job fails due to any type of system failure. A comprehensive log file is generated, so if any simulation cannot be completed, the user will be informed.

5. TOMAS AQUINAS Back End Tools

The TOMAS AQUINAS back-end tools provide the capability to automatically parse the simulation output files, extract the appropriate information, create a reduced data set, perform predefined statistical analyses, and document the simulation parameters, analyses and results.

SimAnalyzer reads the simulation output files, parses the data, and extracts the information specified by the user (e.g. final polarization of the output cell). For each set of Monte Carlo simulation files, SimAnalyzer creates a reduced data file that contains the results of each simulation. This reduced data set is archived and used in subsequent analyses.

ModelExtractor reads the reduced data file and automatically performs a series of user selected statistical analyses. Since the correct output is known a priori, the ModelExtractor applies a user specified threshold to classify each simulation result as correct or incorrect. This transforms the data set into a binomial distribution. Parameters such as the mean and variance are calculated. This data is used to determine the reliability of this gate architecture with this set of process variations and defects.

As the process parameters and defect densities are varied in subsequent batch simulations according to modern design of experiment techniques [15, 16], the data is acquired to generate a predictive model of the behavior of this gate architecture. The model can be utilized in a variety of ways. Given a set of process parameters and reliability requirements, the model can predict the optimum gate architecture. The model automatically identifies the parameters to which the performance of the gate is most sensitive. This information can be used for fabrication process optimization. Also, the model can be used to compare the performance of one gate architecture relative to another.

MATLAB Report Generator is used to automatically document the simulations, analyses and results. An

adaptive template is used to capture the appropriate information. For example, all configuration information entered by the user is always documented. However, as different analyses are selected, the contents of the report are modified to include the analyses and results.

6. Status

A preliminary analysis of the fault tolerance of the ideal majority gate has been completed. Symmetrical rotational errors of up to 45° around the central cell do not affect the performance of the ideal majority gate. Linear translations of the input cells of up to 20 nm away from the gate do not affect the performance of the majority gate. Approximate limits for the linear translation of input cells are still being investigated. The ideal majority gate has been shown to be very sensitive to asymmetrical errors in cell position. Cell alignment errors of less than one-half of a QCA cell side are required. This becomes increasingly difficult as QCA cell dimensions are reduced.

The block majority gate has been shown to be significantly more robust than the ideal majority gate to errors in cell position, missing cells and defective cells. Work is on going to quantitatively determine the improvement in performance and to optimize the performance of the block majority gate.

Software is being developed to expand the capability of AQUINAS. The TOMAS AQUINAS framework integrates the tools to automatically generate and analyze statistical data sets with the AQUINAS simulator. The predictive model that results will enable the optimization of QCA gate architectures and QCA fabrication processes.

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